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Solution-deposited Zr-doped AlO_x gate dielectrics enabling high-performance flexible transparent thin film transistors†

Wooseok Yang,[a] Keunkyu Song,[b] Yangho Jung,[b] Sunho Jeong*[c] and Jooho Moon*[a]

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Although high dielectric constant (*k*) oxide thin film has been considered as a key element for high performance and low-voltage driven thin-film transistors (TFTs), there are no solution processable high-*k* oxide dielectrics that satisfy the stringent requirements of low-temperature processability, mechanical flexibility, and good TFT performance. Here, we demonstrate that the incorporation of a zirconium component that has strong bonding to oxygen enables a significant reduction in the processing temperature for soluble alumina dielectrics to as low as 250 °C. Based on these Zr-AlO_x films, high performance, low operational voltage, flexible TFTs are achieved. Flexible TFTs operate well under a gate bias of 5 V, exhibiting a high saturation mobility of 51 $cm^2 V^{-1} s^{-1}$, an on/off current ratio of 10^4, and a low threshold voltage of 1.2 V with good mechanical flexibility. This is the first study demonstrating the mechanical flexibility of all-oxide soluble high-*k* dielectric–semiconductor-based TFTs with an emphasis on the influence of annealing temperature on the solution-deposited high-*k* oxide dielectric characteristics.

1 Introduction

High-dielectric constant (*k*) inorganic gate dielectrics have received much attention as a key element of thin-film transistors (TFTs) due to their high dielectric constant as well as the coherent interface formation with oxide semiconductors, which lead to considerable improvements in TFT performance.[1] In particular, high performance flexible TFTs are of great interest because of their broad potential applications in wearable, rollable devices and paper-like displays. Since Nomura *et al.* reported flexible oxide TFTs using an amorphous In–Ga–Zn–O (a-IGZO) semiconductor and a Y_2O_3 dielectric in 2004, high performance, low-voltage driven TFTs on polymeric substrates have been developed using several dielectric materials, such as Ta_2O_3 and self-assembled nanodielectric (SAND).[2] However, despite their respectable device performance, especially carrier mobilities that are one or two orders of magnitude higher than those of hydrogenated amorphous silicon (a-Si), those dielectrics possess shortcomings for practical applications because of the necessity of costly vacuum-deposition techniques or layer-by-layer film deposition under an inert gas atmosphere.

To date, low-cost solution processing of high-*k* dielectrics for high performance TFTs has been demonstrated by several groups, showing high carrier mobilities that are comparable to those of polycrystalline Si (*poly*-Si).[1b,3] However, high quality metal-oxide (MO) dielectric films generally require an annealing process at high temperatures above 400 °C, which is undesirable for integrated circuits on flexible substrates by low-cost, high-throughput roll-to-roll processes. Recently, the annealing temperature for solution-processed oxide semiconductors has been lowered drastically through the adoption of diverse chemically assisted annealing methods, but the processing strategies for soluble dielectric materials are still demanding.[4] Low-temperature fabrication of high quality MO dielectrics by solution processing is a key issue in this emerging field. However, most studies, including the recent development of solution-processed, low-temperature (300 °C) annealed aluminum oxide and hafnium oxide dielectrics,[1c,5] have mainly focused on the simple demonstration of TFTs without a systematic study of the relationship between the annealing temperature for the formation of the MO dielectric layer and the TFT device performance. In developing noble materials that meet the low-temperature processability requirement as well as the physical/electrical requirements, an understanding of the temperature-dependent evolution of the oxide framework that critically influences the electrical characteristics of oxide gate dielectrics is of significant importance.

[a]Department of Materials Science and Engineering, Yonsei University, 50 Yonsei-ro Seodaemun-gu, Seoul 120-749, Republic of Korea. E-mail: jmoon@yonsei.ac.kr

[b]LCD R&D Center, Samsung Electronics Co. LTD., Gyeonggi-do 449-711, Republic of Korea

[c]Advanced Materials Division, Korea Research Institute of Chemical Technology (KRICT), Daejeon 305-600, Republic of Korea. E-mail: sjeong@krict.re.kr

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The fundamental challenge in depositing oxide dielectrics from a precursor solution is associated with the conversion of the soluble precursors into metal-oxide films.[6] After the solution deposition, the films should be subjected to a high annealing temperature above 400 °C for the removal of residual organic species, for oxide lattice formation *via* dehydration, dehydroxylation, and polycondensation, and for densification and occasional crystallization.[7] During this chemical reaction for oxide lattice formation, undesirable defects such as metal hydroxide, oxygen vacancies, and organic impurities are generated. Note that these internal defects and grain boundaries act as a pathway for leakage current.[8] In this regard, the annealing temperature is a crucial factor in determining the electrical characteristics of the dielectric layers. When annealed at low temperatures, the presence of lattice defects and organic impurities makes the dielectric layer too leaky and consequently keeps the TFTs in a "normally on" state. High temperature annealing leads to the formation of grain boundaries through crystallization. Therefore, a desirable gate dielectric should exhibit a low oxide-formation temperature and a high crystallization temperature. It has been reported that, for solution-processed oxide semiconductors, the formation of an oxide lattice with fewer lattice defects can be facilitated by incorporating a dopant that has a high bond strength with oxygen. For example, the doping of gallium plays a prominent role in diminishing the relative density of both metal hydroxides and oxygen vacancies.[9] Furthermore, the dielectric properties of the binary metal-oxide high-*k* gate dielectric can be improved by adding a third element into the dielectric.[10] Adding a suitable dopant also hinders the amorphous-to-crystallization transition, as the original bond structure order is distorted.[11]

Zirconium oxide (ZrO_2) is well-known as a highly polarizable material, so it has an appreciably high dielectric constant. However, ZrO_2 tends to exhibit a low breakdown voltage and a higher leakage current density. In contrast, Al_2O_3 is an attractive material in terms of a high breakdown field but has a relatively low dielectric constant.[12] Herein, we report a novel solution-processed gate dielectric, which is compatible with polymeric flexible substrates, by combining highly insulating aluminum oxide with a highly polarizable zirconium component that has strong bonding to oxygen. We demonstrate that the process temperature for soluble oxide gate dielectrics can be reduced to as low as 250 °C, enabling high performance, flexible TFTs. The flexible TFTs, which are fabricated by coupling a Zr-doped aluminum oxide gate dielectric with a soluble n-type oxide semiconductor, exhibit excellent operating characteristics under a gate bias of 5 V, with an exceptionally high saturation mobility of 51 $cm^2 V^{-1} s^{-1}$, an on/off current ratio of 1.8×10^4, and a low threshold voltage (V_T) of 1.2 V.

2 Experimental

2.1 Precursor solution synthesis

AlO_x and ZAO solutions were synthesized using aluminum chloride ($AlCl_3$, Aldrich, 99.99%) and zirconium chloride ($ZrCl_4$, Aldrich, 99.9%), respectively. The precursors were dissolved in 7 ml of acetonitrile (CH_3CN, Duksan Pure Chemical, 99.5%) and 13 ml of ethylene glycol (Aldrich, 99.8%). The total concentration of the precursor in the solution was 0.4 M, and the molar composition ratio of the ZAO precursor solution was Zr/Al = 10/90. The ratio of Zr and Al was optimized for obtaining high-*k* and low leakage dielectric films by annealing at 250 °C. The precursor solution for IZO was synthesized using zinc nitrate hexahydrate ($Zn(NO_3)_2 \cdot 6H_2O$, Aldrich, 98%) and indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$). An IZO solution with a 0.2 M concentration was prepared in 2-methoxyethanol (Aldrich, 99.8%), and the molar composition ratio of the IZO precursor solution was In/Zn = 70/30. The 0.1 M aqueous ZnO solutions were prepared by directly dissolving zinc hydroxide ($Zn(OH)_2$ Junsei, 98%) in an aqueous ammonia solution (NH_4OH, Alfa Aesar, 25%), resulting in a clear solution with a pH of 13.5.[4d] For the gate electrodes on transparent glass, 0.2 M of ITO solutions were synthesized by dissolving tin acetate ($Sn(CH_3COO)_4$, Aldrich) and indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$, Aldrich, 99.9%) in 2-methoxyethanol. The molar composition ratio of In/Sn was fixed at 95/5.[13]

2.2 Device fabrication

The AlO_x and ZAO precursor solutions were separately spin-coated onto a heavily doped p^{++} Si wafer at 4000 rpm for 25 s and dried at 120 °C for 2 min and were then annealed at the desired temperature for 2 h. This process was repeated several times to obtain an appropriate thickness. To estimate the electrical characteristics of the gate dielectric, a 50 nm thick Au dot electrode was deposited by thermal evaporation on either the ZAO- or the AlO_x-coated heavily doped p^{++} Si substrate. To fabricate the TFTs with a bottom-gate top-contact configuration, ZAO solutions were spin-coated onto a heavily doped p^{++}-type Si wafer, a spin-coated ITO gate/glass substrate, or a vacuum-deposited ITO/PI (t = 50 μm) substrate. The ITO solution was spin-coated at a speed of 2500 rpm for 25 s onto a glass substrate and was then annealed at 350 °C for 2 h on a hot plate. After the ZAO films were treated in a UV oven for 30 min to eliminate contamination and to improve wettability for the semiconductor solutions, the semiconductor solutions were coated at either 3000 rpm (IZO) or 2000 rpm (ZnO) for 25 s. The coated IZO and ZnO layers were annealed at the same temperature as the dielectric films. The annealing steps were carried out using a hot plate, except for the flexible TFTs, which were treated in a convection oven (BPG-9050A, Neuron Fit Co., Ltd.). Subsequently, the aluminum source and drain electrodes with 50 nm thicknesses were deposited by thermal evaporation through the shadow mask to fabricate top-contact transistors. The channel width (W) and length (L) were 3000 μm and 100 μm, respectively.

2.3 Characterization

The capacitance–voltage (C–V) characteristics at varying frequencies were measured using an Agilent E4980A LCR meter, while the leakage current–voltage (I–V) characteristics and TFT characteristics were measured using an Agilent 4155C semiconductor parameter analyzer. The saturation mobility (μ_{sat}), subthreshold slope (S), and interface trap density (D_{it}) were

calculated using the conventional metal-oxide-semiconductor field effect transistor (MOSFET).[14] The crystallization and structural information were obtained using high-resolution X-ray diffractometry with CuK_α radiation (X PET-PRO MRD, Phillips). The cross-sectional microstructures of the ZAO and ZAO-based TFTs were investigated using high-resolution transmission electron microscopy (HR-TEM, JEM-2100F, JEOL). The film thicknesses were determined by a spectroscopic ellipsometer (SE MG-Vis 1000, Nano-view) and were further confirmed using field emission scanning electron microscopy (FE-SEM, JEOL JSM-6700F). Surface analyses of the AlO_x and ZAO were performed using atomic force microscopy (AFM, SPA 400, SEIKO) and XPS (Escalab 220i-XL, Thermo VG, U.K.) using Al twin anode X-ray sources (Al K_α line: 1486.6 eV), and the optical properties of the ZAO-based TFTs on glass were measured using a UV-vis spectrophotometer (V-530, JASCO).

3 Results and discussion

To quantify the dielectric properties of the undoped AlO_x and the Zr-doped AlO_x (ZAO), metal–insulator–semiconductor (MIS) sandwich structure devices were fabricated with a thermally evaporated Au electrode and a p^{++} Si substrate. Each thin film was spin-coated from the precursor solutions, followed by annealing at temperatures ranging from 350 °C to as low as 250 °C. As shown in Fig. 1a and b, the leakage current density of AlO_x films increases as the annealing temperature drops. The high leakage current densities of AlO_x at low temperatures ($>10^{-4}$ A cm^{-2} at 2 MV cm^{-1} at 250 °C) are inadequate for TFT operation. In contrast, ZAO films exhibit a low leakage current density ($<10^{-6}$ A cm^{-2} at 2 MV cm^{-1}) even when they are annealed at 250 °C, which is acceptable for stable TFT operation. The improved leakage characteristics of ZAO are attributed to the higher bond strength of Zr–O (776.1 kJ mol^{-1}) as compared to that of Al–O (511 kJ mol^{-1}).[15] The schematics showing the conceptual structural features of AlO_x and ZAO are illustrated in Fig. 1c and d. The solution-deposited amorphous alumina thin films contain the lattice defects and hydroxides due to their weak bonding to oxygen. However, when the weakly bonded oxygen was replaced with strongly bonded oxygen upon the addition of a Zr cation, an oxide framework with fewer lattice defects and hydroxides was generated. For the O1s peak obtained from the XPS spectrum (Fig. 2), the near-Gaussian peak at 529.5 ± 0.5 eV indicates well-bonded oxygen, whereas the peak at 531 ± 0.5 eV implies the oxygen atom that is associated with lattice defects such as oxygen vacancies, metal vacancies, and/or interstitials adjacent to the oxygen in the lattice structure. The feature at ~532.0 eV is assigned to the oxygen in the hydroxide due to highly electronegative hydrogen atoms. The peak for chlorate, which comes from the precursor (aluminum and zirconium chloride), is located at ~533 eV.[9a,16] The reported role of halogenide derivatives in high-k materials such as HfO_2 is reducing fixed charges and/or passivating interface traps, which leads to the improvement of TFT performance.[17] It is clearly observed that the peak areal fraction for thermally activated oxides increases as the processing temperature goes up, whereas that for hydroxide decreases. The detailed position, full-width-at-half-maximum (FWHM), and areal fraction of each sub-peak for both AlO_x and ZAO films are summarized in Table S1 (ESI†). The XPS results revealed that the incorporation of zirconium ions facilitates the oxide lattice formation in the AlO_x film at a low temperature.

Capacitance–frequency (C–f) measurements were carried out on the same metal–insulator–semiconductor (MIS) structures employing the AlO_x and ZAO gate dielectric layers annealed at

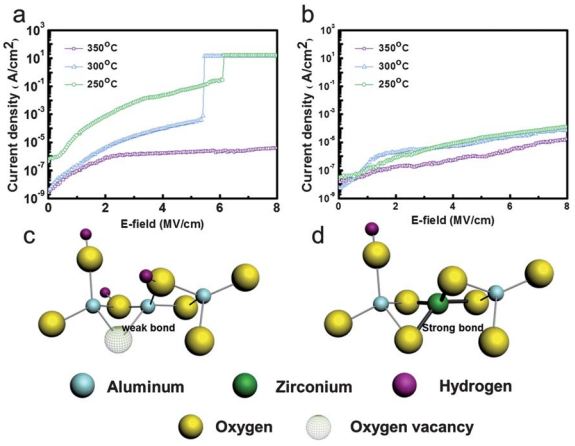

Fig. 1 Effect of zirconium doping on the electrical properties of the solution-processed amorphous alumina thin film. Leakage current density *vs.* electric field plots for (a) AlO_x and (b) ZAO. Schematics showing the conceptual structural features of (c) AlO_x and (d) ZAO. AlO_x contain weakly bonded oxygen-associated lattice defects or hydroxide due to their weak bonding to oxygen, which are replaced with strongly bonded oxygen upon the addition of a Zr cation.

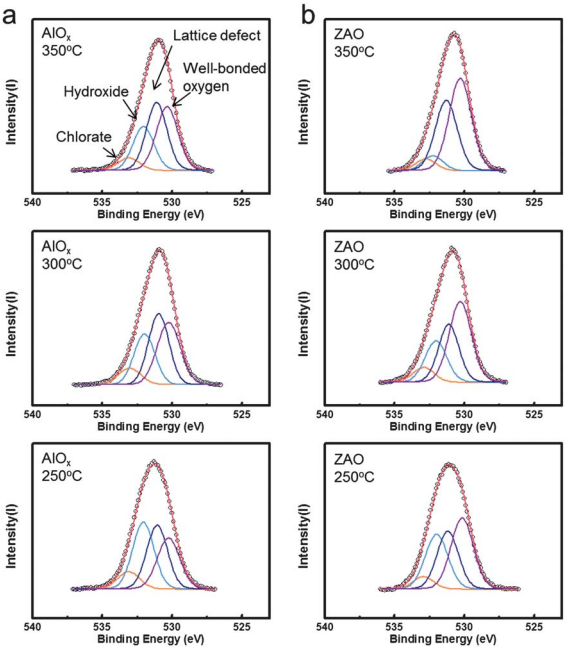

Fig. 2 O1s XPS spectra for (a) AlO_x and (b) ZAO films annealed at the indicated temperature. The three peaks originate from well-bonded oxygen (~530.2 eV), lattice defect (~531.1 eV), hydroxide (~532 eV) and chlorate (~533 eV) respectively.

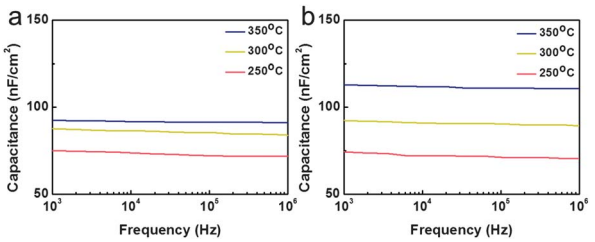

Fig. 3 Capacitance *vs.* frequency plots for (a) AlO_x and (b) ZAO films annealed at the indicated temperature.

different temperatures (Fig. 3). Although the capacitance increases slightly as the frequency decreases, the difference between the capacitances at 1 MHz and at 1 kHz is less than five percent for all of the films. The capacitance, thickness, and calculated dielectric constant of each film are summarized in Table 1. The calculated dielectric constant of ZAO (8.4–11.8) is higher than that of AlO_x (5.6–6.2). The relatively low dielectric constants of solution-derived oxides with respect to the corresponding stoichiometric crystalline counterparts (*e.g.*, k (Al_2O_3) ~9) are mainly due to the presence of small amounts of organic residues, slightly incomplete oxide lattice formation, and partial densification when annealed below 350 °C.[1c,18] The dielectric constant for ZAO films increased more steeply depending on annealing temperatures, compared with AlO_x films. The aluminum hydroxide has a lower dielectric constant than AlO_x and ZrO_x; thus, the high temperature-dependent behavior of dielectric constant for ZAO films can be correlated with the more effective conversion of hydroxyl groups to oxide lattices. As the annealing temperature increased from 250 °C to 350 °C, the ϕ_{oxide} (the ratio of oxide lattice to hydroxyl group in the XPS spectrum at a given temperature) for ZAO films considerably increased by 5.32 (from 1.28 to 6.6) whereas ϕ_{oxide} for AlO_x films increases by only 0.69 (from 0.81 to 1.5).

Bottom-gate, top-contact configuration TFTs were fabricated using a ZAO layer and a soluble n-type oxide semiconductor such as InZnO (as a polar solvent-based solution) or ZnO (as an aqueous precursor solution), which have been previously reported by our group (Fig. 4a). The cross-sectional TEM images revealed an entirely amorphous, dense, 95 nm thick ZAO dielectric layer without any pores or cracks. These excellent morphological characteristics of the ZAO dielectric indicate that there is no current path through the morphological defect sites. There are two interfaces in the ZAO layer, which might result

Table 1 Annealing temperature (T_a), capacitance, film thickness, and calculated dielectric constant data for the metal–insulator–semiconductor (MIS) structure fabricated using AlO_x and ZAO

Sample	T_a (°C)	Capacitance at 1 MHz (nF cm^{-2})	Thickness (nm)	Dielectric constant
AlO_x	250	71	70	5.6
	300	84	64	6.1
	350	91	61	6.2
ZAO	250	70	106	8.4
	300	90	100	10.2
	350	110	95	11.8

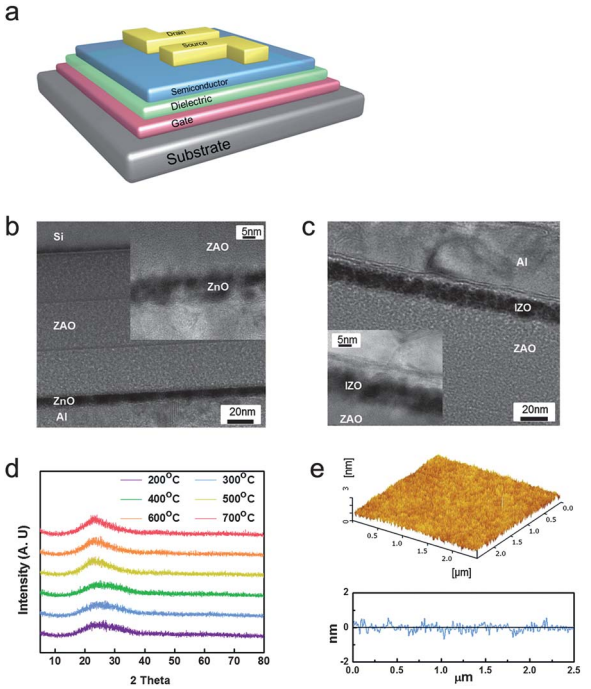

Fig. 4 Structural and surface properties of ZAO. (a) Schematic of top-contact bottom-gate TFT device configuration used in this study. High resolution cross-sectional TEM images of ZAO-based TFTs with either (b) ZnO channel or (c) IZO channel, showing a high-quality ZAO film and smooth interface with channel. (d) XRD results for the ZAO film annealed at temperatures ranging from 200 to 700 °C. (e) Atomic force microscopy (AFM) surface roughness of the ZAO film annealed at 350 °C.

from the surface carbon that remains after the first and second annealing processing steps. The organic residues inhibit the homogenous chemical reaction at each interface.[5] The amorphous nature of the ZAO films was further confirmed by an X-ray diffraction (XRD) analysis (Fig. 4d). The ZAO films were identified as an amorphous phase up to the annealing temperature of 700 °C. A smooth gate dielectric/semiconductor interface is a prerequisite for expeditious charge carrier mobility in the TFT channel.[19] Fig. 4e shows the AFM image of the ZAO annealed at 350 °C, suggesting that the ZAO films have a smooth surface with a root-mean-square (rms) roughness of 0.22 nm. The highly-coherent interfaces between the ZAO dielectric and either IZO or ZnO semiconductors are shown in Fig. 4b and c (inset). The RMS roughness of the IZO/ZAO (0.51 nm) and ZnO/ZAO (0.6 nm) stacks (see, Fig. S1 in the ESI†) implies a morphologically compatible semiconductor/dielectric interface, which can improve the current channel quality.

The electrical characteristics of the present ZAO-based TFTs with semiconducting IZO and ZnO films were first evaluated on a heavily doped p^{++}-type Si substrate (gate) with thermally evaporated 50 nm thick Al source and drain electrodes (3000 μm in width and 100 μm in length). The device response parameters are summarized in Table 2. Fig. 5a and d show the I_{DS}–V_G transfer characteristics and I_{DS}–V_{DS} output characteristics, respectively, of IZO transistors employing the ZAO-dielectric. Both the IZO and ZAO layers were annealed at 350 °C. The I_{DS}–V_{DS} graph shows clear linear and saturation regions in the

Table 2 Component materials and device performance parameters of oxide TFTs with aluminum source–drain and W/L ratio = 30

Substrate/gate	Semi-conductor type	T_a[a] (°C)	μ_{sat} ($cm^2\ V^{-1}\ s^{-1}$)	On/off	V_T (V)	S (V per decade)	Interfacial trap density ($cm^{-2}\ eV^{-1}$)
p^{++} Si	IZO	350	53	1.26×10^6	1.07	0.12	6.55×10^{11}
p^{++} Si	IZO	250	12	1.9×10^4	2.46	0.71	4.79×10^{12}
p^{++} Si	ZnO	350	48.9	7.52×10^5	1.42	0.25	2.02×10^{12}

[a] T_a = annealing temperature.

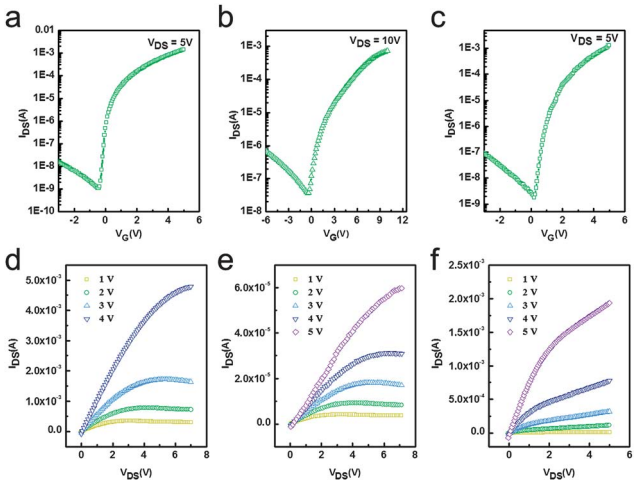

Fig. 5 Transfer characteristics (I_{DS} *versus* V_G) and output characteristics (I_{DS} *versus* V_{DS}) for ZAO-based transistors with a 3000 μm channel width and 100 μm channel length. (a–c) Transfer characteristics of (a) IZO/ZAO/p^{++} Si annealed at 350 °C, (b) IZO/ZAO/p^{++} Si annealed at 250 °C, and (c) ZnO/ZAO/p^{++} Si annealed at 350 °C. (d–f) Output characteristics corresponding to the above transfer curves.

output characteristics. The parameters governing the TFT performance include the saturation mobility (μ_{sat}), current on/off ratio (I_{on}/I_{off}), and subthreshold swing (S). These parameters define the drift velocity of the charge carrier in the channel from the source to the drain with a high drain voltage, the current modulation between the TFT "on" and "off" states, and the inverse of the maximum slope of the transfer characteristic indicating the necessary V_G to increase I_{DS} by one decade.[20] A high saturation-regime mobility of ~53 $cm^2\ V^{-1}\ s^{-1}$ was measured with a high on/off ratio of 10^6 and a good S value of 0.12 V per decade. Because we used a non-patterned IZO channel layer, some peripheral currents caused by the fringing electric field outside the channel could result in overestimated drain currents and mobilities.[21] However, the fringing electric field effects on the TFT performance metrics could be negligible due to the large W/L ratio of 30.[22]

We believe that our device shows a high gate leakage current owing to the non-patterned channel layer, which is nothing to do with the quality of dielectric films. To verify it, we carried out further experiments by measuring electrical characteristics of TFTs employing the patterned channel layer (Fig. S3a, ESI†). Ink jet printing of IZO solution on the ZAO gate dielectric allowed the formation of a patterned channel layer of 1000 μm in width and 100 μm in length. The thickness of the channel layer was 12 nm. The confocal image of printed IZO channel TFTs is shown in Fig. S3b (ESI†). The device characteristic of the ink-jet printed channel based TFTs was measured to be comparable to that of the spin-coated channel (*i.e.*, non-patterned) based transistor, even exhibiting much lower gate leakage current by a factor of 1000 (Fig. S2 and Fig. S3a, ESI†). The patterned channel device exhibits a high mobility of ~54.2 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio of 5×10^4, and threshold voltage of 1.47 V, whereas the non-patterned channel device exhibits a mobility of ~53 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio of 1.26×10^6, and threshold voltage of 1.07 V. The on-current level of the printed IZO-based transistor is lower than that of the spin-coated IZO transistor due to the narrow channel width. This observation supports that the non-patterned channel layer does not contribute to an overestimation of the mobility.

Thus, it is speculated that the high mobility and low operating voltage are attributed to the smooth dielectric/semiconductor interface (as confirmed by the TEM and AFM images), the low interface trap density as calculated from the subthreshold value (6.55×10^{11} $cm^{-2}\ eV^{-1}$, see the Experimental section), and the high capacitance of the ZAO dielectric layer. This high mobility is comparable to the recently reported high performance TFTs using solution-deposited Li–ZnO/ZrO_2 (85 $cm^2\ V^{-1}\ s^{-1}$)[1b] and ZnSnO/AlO_x (33 $cm^2\ V^{-1}\ s^{-1}$).[1c] IZO/ZAO TFTs were also fabricated at 250 °C with identical device architecture and dimensions, and the device performance is shown in Fig. 5b and e. The IZO TFTs with the ZAO dielectric annealed at 250 °C require an operating voltage of 10 V, which is higher than that of the TFTs employing the 350 °C-annealed ZAO dielectric layer due to the relatively low capacitance of the ZAO layer annealed at 250 °C (Fig. 3). To investigate the interfacial versatility of the ZAO dielectric, aqueous solution-based ZnO channel TFTs were also fabricated at 350 °C on a heavily doped silicon substrate (Fig. 5c and f). The ZnO TFTs showed a high saturation mobility of 48.9 $cm^2\ V^{-1}\ s^{-1}$ and an on-to-off current ratio of 7.5×10^5. The aqueous solution-based ZnO semiconductor acts well as a high-performance channel layer by annealing below 200 °C on robust, thermally oxidized SiO_2 gate dielectrics in our preliminary study.

However, the ZnO-based TFTs that employ the soluble ZAO layer annealed below 300 °C did not operate well due to chemical attack by ammonium hydroxide in the aqueous ZnO precursor solution, which degrades the quality of the interface and the insulating properties of the ZAO dielectric layer (Fig. S4, ESI†). With the present successful integration of ZAO dielectric-based TFTs, we also demonstrated all-solution-processed all-oxide TFTs on a transparent glass substrate combining a solution-deposited conductive indium tin oxide (s-ITO) (see the

Experimental section), ZAO dielectric, and an aqueous solution-based ZnO semiconductor. All of the layers (s-ITO, ZAO, and ZnO) were annealed at 350 °C. This device showed high optical transparency (T) in the visible region (T > 80%, Fig. 6c and d) and exhibited a high mobility of 32.3 $cm^2\ V^{-1}\ s^{-1}$ and an on/off current ratio of 8×10^5 (Fig. 6a and b).

Another novelty of our study is demonstrating the feasibility of flexible TFTs, which has not been previously reported for TFTs with stacks of soluble oxide gate dielectric and soluble oxide semiconductor. The TFTs using a solution-deposited ZAO dielectric and an IZO channel were fabricated next on sputtered ITO/polyimide (PI) substrates with Al source–drain electrodes. The annealing temperature for the IZO semiconductor and ZAO dielectric is optimized at 280 °C in a convection oven in order to achieve maximum device performance and to prevent substrate deformation due to thermal stress. To investigate the mechanical properties of the ZAO-based flexible TFTs, we performed bending tests in the longitudinal direction (where the channel direction is oriented parallel to the bending direction) by measuring the electrical characteristics of the devices while wrapped around glass vials with different radii, as shown in Fig. 7a. The ZAO-based flexible TFTs exhibited a high mobility of 51 $cm^2\ V^{-1}\ s^{-1}$, an on/off current ratio of 1.8×10^4, a low threshold voltage of 1.2 V, and a small counter-clockwise hysteresis. In principle, the hysteresis direction and magnitude can be attributed to the following mechanisms: (1) charge traps at the channel/dielectric interface, (2) slow polarization in the dielectric layer, (3) mobile charges, and (4) charges injected from the gate electrode.[2b,23] The electronic polarization is fast enough to respond with a gate voltage sweep in general TFT operations, but the polarization of the polar group, mainly the hydroxyl group in a ZAO gate dielectric layer, leads to additional charge accumulation during the reverse gate sweep due to slow orientation along the gate bias, resulting in a counter-clockwise hysteresis. For low-temperature annealed, solution-processed oxides, the incomplete thermal decomposition of organic impurities is unavoidable during the thermally activated evolution of oxide lattices, which leaves behind mobile charge species that move slowly inside a gate dielectric under the electric field. This mobile charge acts as another source for the counter-clockwise hysteresis, as does a chemical moiety with slow polarization. In addition, the hydroxyl group is a well-known site for the trapping of electrons, and a positively charged oxygen vacancy is also a trap site for electrons; thus, the electrons injected from a gate electrode are trapped inside a gate dielectric, causing clockwise hysteresis. Therefore, the counter-clockwise hysteresis in our high-k based TFTs is believed to be affected predominantly by both slow polarization and mobile charge carriers over both of the charge traps at the SiO_2/IZO interface and the charges injected from the gate electrode. However, as shown by a small threshold voltage shift in the hysteresis behavior, the contributions of both the slow polarization and mobile charge carriers are negligible. In contrast, the slightly clockwise hysteresis observed for SiO_2-based TFTs (Fig. S5 in the ESI†) is related to the charge traps at the SiO_2/IZO interface. Since the thermally oxidized SiO_2 dielectrics have very few hydroxyl groups, oxygen vacancies, and chemical impurities, the counter-clockwise hysteresis caused by these chemical factors can be excluded. Fig. 7c shows the transfer characteristics and I_{DS}–V_G plots of identical devices that were tested before, during, and after bending, and the performance parameters are compiled in Table 3. The device performance parameters were evaluated at the calculated strains of 0.2% and 0.36%, which correspond to bend radii of 12 and 7 mm, respectively. When the device was in the bent position, I_{on} decreased slightly from 1.2×10^{-3} A to 2.8×10^{-4} A, along with a slight decrease in μ_{sat}, while I_{off} increased slightly. The degraded characteristics of the TFTs in bent positions, including the decrease in I_{on} and the increase in I_{off}, can be attributed to strain-induced defects in the semiconductor and dielectric layer.[24] Although the bending caused decreases in both μ_{sat} and the on/off current ratio, the device performance

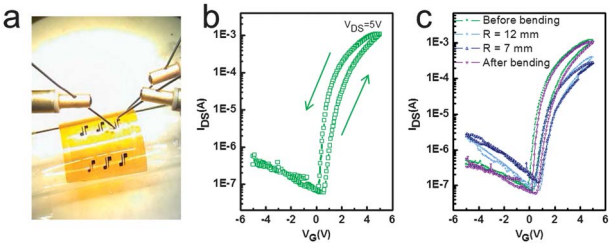

Fig. 7 Transfer characteristics (I_{DS} *versus* V_G) of ZAO-based transistors on an ITO/PI substrate with a 3000 μm channel width and 100 μm channel length. (a) Optical image of an array of TFTs with ZAO dielectric on an ITO/PI substrate, wrapped around a test tube with a radius of 7 mm during measurement. (b) Transfer characteristics of TFTs in a flat position. (c) Transfer characteristics of TFTs tested before, during, and after bending.

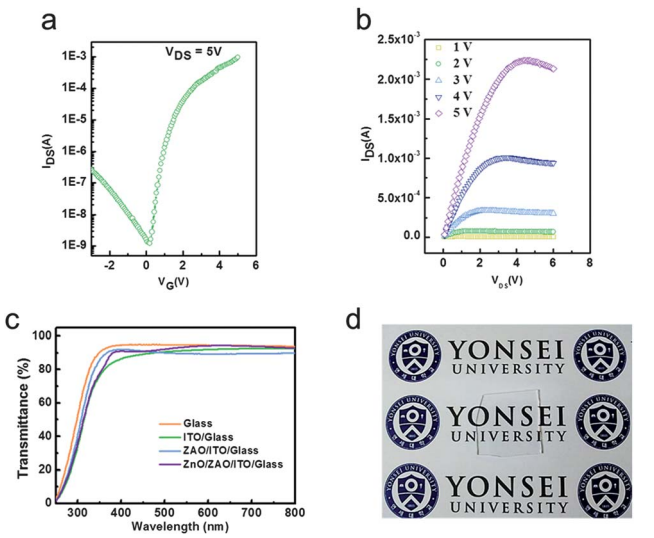

Fig. 6 Electrical and optical characteristics for ZAO-based transistors on a transparent substrate. (a) Transfer characteristics (I_{DS} *versus* V_G) and (b) output characteristics (I_{DS} *versus* V_{DS}) for aqueous ZnO TFTs on ZAO/s-ITO/glass annealed at 350 °C with a 3000 μm channel width and 100 μm channel length. (c) Optical transmission spectra of bare glass substrate, s-ITO/glass, ZAO/s-ITO/glass and ZnO/ZAO/s-ITO/glass. (d) Photograph of the transparent device after successive depositions of s-ITO, ZAO, and ZnO layers on a glass substrate.

Table 3 Device parameters for the flexible TFTs tested before, during, and after bending along a curvature parallel to the channel length

	ε_r[b] (%)	μ_{sat} ($cm^2\ V^{-1}\ s^{-1}$)	On/off ratio	V_T (V)
Before bending		51	1.8×10^4	1.3
Bending, $r^a = 12$ mm	0.2	30.3	4.0×10^3	2
Bending, $r = 7$ mm	0.36	21.2	2.3×10^3	1.8
After bending		50.2	1.4×10^4	1.1

[a] r = bending radius. [b] ε_r = tensile strain, calculated from $\varepsilon_r \approx d_s/2r$, where d_s is the substrate thickness (= 50 μm for polyimide used in this study).

almost completely recovered after the strain was relaxed. The degradation and recovery of the flexible transistor performance have been observed in several studies regarding carbon nanotubes, Si nanoribbons, and organic/inorganic transistors.[2c,16,25]

4 Conclusions

We have demonstrated here that a new soluble ZAO gate dielectric using highly insulating aluminum oxide and highly polarizable zirconium oxide affords a smooth, dense, amorphous, pinhole-free dielectric layer. The incorporation of a zirconium component that has strong bonding to oxygen allowed for an unprecedented soluble high-k dielectric that enables a significant reduction in the processing temperature to as low as 250 °C. High performance TFTs were fabricated by combining an n-type soluble semiconductor (either IZO or ZnO) with the ZAO dielectric on diverse substrates including p^{++} Si, transparent glass, and a flexible polymeric substrate. The flexible devices exhibited a high μ_{sat} of ~51 $cm^2\ V^{-1}\ s^{-1}$ with $I_{on}/I_{off} \sim 10^4$ and $V_T \sim 1.3$ V. Furthermore, these flexible devices were characterized under mechanical tensile strain. Although the device performance was degraded slightly in bent positions, the performance almost completely recovered. Our finding provides potential for realizing low-cost fabrication of high-speed, low-power flexible devices.

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